REMARKS/ARGUMENTS

Claims 1-31 are pending in this application. The Examiner has allowed claims 1-23. The Examiner has rejected claims 24-29 and objected to claims 30 and 31. Applicant respectfully requests reconsideration of pending claims 24-31.

The Examiner has rejected claims 24, 28, and 29 under 35 U.S.C. § 102(b) as being anticipated by Kobayashi in U.S. Patent No. 4,775,974. Applicant respectfully disagrees.

Regarding claim 24, Applicant submits the cited reference fails to disclose the features of claim 24. For example, Applicant submits the cited portions of the cited reference fail to disclose a method for processing ingress data units in a link layer processor of a multiprocessor control block in a communication switch, comprising: receiving a first ingress data unit corresponding to a call; selecting a first selected intermediate processor of a plurality of intermediate processors included in the multiprocessor control block; and forwarding the first ingress data unit to the first selected intermediate processor. Applicant notes col. 3, lines 22-26, of Kobayashi states, "Link layer processor 21 is connected to demultiplexer 23 where outgoing frames are individually separated according to their destinations for coupling to packet layer processors 24-1 to 24-n." Applicant submits link layer processor 21 does not appear to perform the steps of selecting a first selected intermediate processor of a plurality of intermediate processors included in the multiprocessor control block or forwarding the first ingress data unit to the first selected intermediate processor. Moreover, Applicant notes the quote above from Kobayashi recites "outgoing frames," not "a first ingress data unit." Thus, Applicant submits the cited portions of the cited reference fail to disclose the subject matter of claim 24. Therefore, Applicant submits claim 24 is in condition for allowance.

Regarding claims 28 and 29, Applicant submits the cited reference fails to disclose the features of claims 28 and 29. For example, Applicant submits the cited portion of the cited reference fails to disclose assigning a sequence number to the first ingress data unit, wherein the sequence number corresponds to the call. Rather, the Examiner cites different features of different elements of the cited reference. The Examiner cites col. 4, lines 29-33 and 39-42, which relate, respectively, to an error detector 61 of link layer processor 21 and a frame sequence number generator 65 of link layer processor 21 but then cites col. 5, lines 34-39, which relate to a header updating circuit 76 of packet layer processor 24. Applicant submits, based on the teachings of the cited portions of the cited

reference, the functionality of the error detector 61 and/or frame sequence number generator 65 of link layer processor 21 cannot be imputed to header updating circuit 76 of packet layer processor 24, nor can the functionality of the header updating circuit 76 of packet layer processor 24 be imputed to error detector 61 and/or frame sequence number generator 65 of link layer processor 21. Thus, Applicant submits the cited portions of the cited reference fail to disclose the features of claims 28 and 29. Therefore, Applicant submits claims 28 and 29 are in condition for allowance.

As another example, with respect to claim 29, Applicant submits the cited portions of the cited reference fail to disclose receiving a second ingress data unit corresponding to the call; assigning the sequence number corresponding to the call to the second ingress data unit; selecting a second selected intermediate processor of the plurality of intermediate processors; and forwarding the second ingress data unit to the second selected intermediate processor. Applicant again notes col. 3, lines 22-26, of Kobayashi, which states, "Link layer processor 21 is connected to demultiplexer 23 where outgoing frames are individually separated according to their destinations for coupling to packet layer processors 24-1 to 24-n." Accordingly, Applicant submits the cited portion of the cited reference appears to fail to teach receiving a second ingress data unit corresponding to the call;...and forwarding the second ingress data unit to the second selected intermediate processor. Thus, Applicant submits claim 29 is in condition for allowance.

The Examiner has rejected claims 25-27 under 35 U.S.C. § 103(a) as being unpatentable over Kobayashi in U.S. Patent No. 4, 775,974 in view of Tzeng in U.S. Patent No. 6,438,135. Applicant respectfully disagrees.

Regarding claim 25, the Examiner acknowledges, "KOBAYASHI differs from the claim, in that, it fails to disclose the selection of the first selected intermediate processor based on a prioritization scheme...." Applicant submits both the Kobayashi and Tzeng references, either alone or in combination, fail to anticipate or render obvious the features of claim 25. For example, Applicant submits the Kobayashi reference teaches away from the aspects of teachings of Tzeng alleged by the Examiner. Applicant again notes col. 3, lines 22-26, of Kobayashi, which states, "Link layer processor 21 is connected to demultiplexer 23 where outgoing frames are individually separated according to their destinations for coupling to packet layer processors 24-1 to 24-n." As Applicant submits Kobayasi expressly teaches the outgoing frames (not ingress data units) are "individually separated according to their destinations," Applicant submits Kobayashi teaches away from wherein selecting the first selected intermediate processor further comprises selecting the first selected intermediate

processor based on a prioritization scheme. Moreover, as Applicant has noted, Applicant submits link layer processor 21 does not appear to perform the steps of selecting a first selected intermediate processor of a plurality of intermediate processors included in the multiprocessor control block. Thus, Applicant submits the cited portions of the cited references, either alone or in combination, fail to anticipate or render obvious the features of claim 25. Therefore, Applicant submits claim 25 is in condition for allowance.

Regarding claims 26 and 27, the Examiner acknowledges, "Kobayashi differs from the claim, in that, it fails to disclose the prioritization scheme includes a round robin scheme and at least partially based on loading on each intermediate processor of the plurality of intermediate processors...." Applicant submits both the Kobayashi and Tzeng references, either alone or in combination, fail to anticipate or render obvious the features of claims 26 and 27. For example, Applicant submits the Kobayashi reference teaches away from the aspects of teachings of Tzeng alleged by the Examiner. Applicant again notes col. 3, lines 22-26, of Kobayashi, which states, "Link layer processor 21 is connected to demultiplexer 23 where outgoing frames are individually separated according to their destinations for coupling to packet layer processors 24-1 to 24-n." As Applicant submits Kobayasi expressly teaches the outgoing frames (not ingress data units) are "individually separated according to their destinations," Applicant submits Kobayashi teaches away from wherein selecting the first selected intermediate processor further comprises selecting the first selected intermediate processor based on a prioritization scheme and further teaches away from wherein the prioritization scheme includes a round robin scheme or wherein the prioritization scheme is at least partially based on loading on each intermediate processor of the plurality of intermediate processors. Moreover, as Applicant has noted, Applicant submits link layer processor 21 does not appear to perform the steps of selecting a first selected intermediate processor of a plurality of intermediate processors included in the multiprocessor control block. Thus, Applicant submits the cited portions of the cited references, either alone or in combination, fail to anticipate or render obvious the features of claims 26 and 27. Therefore, Applicant submits claims 26 and 27 are in condition for allowance.

As another example, with respect to claim 27, Applicant notes can find no teaching in col. 4, lines 49-57 of the Tzeng reference, as cited by the Examiner, of wherein the prioritization scheme is at least partially based on loading on each intermediate processor of the plurality of intermediate processors. Thus, even if an attempt were made to combine the teachings of the cited portions of the cited references, Applicant submits such attempt would not yield the features recited in claim 27.

Thus, Applicant submits claim 27 remains nonobvious over the cited portions of the cited references, either alone or in attempted combination. Therefore, Applicant submits claim 27 is in condition for allowance.

The Examiner has allowed claims 1-23. The Examiner has objected to claims 30 and 31 but states they would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant has presented arguments for the allowability of at least one claim from which claims 30 and 31 depend. Thus, Applicant submits claims 30 and 31 are also in condition for allowance.

In conclusion, Applicant has overcome all of the Office's rejections, and early notice of allowance to this effect is earnestly solicited. If, for any reason, the Office is unable to allow the Application on the next Office Action, and believes a telephone interview would be helpful, the Examiner is respectfully requested to contact the undersigned attorney.

Respectfully submitted,

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Date

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